

# TETRODE BOARD GRID 2 SHUNT REGULATED SUPPLY

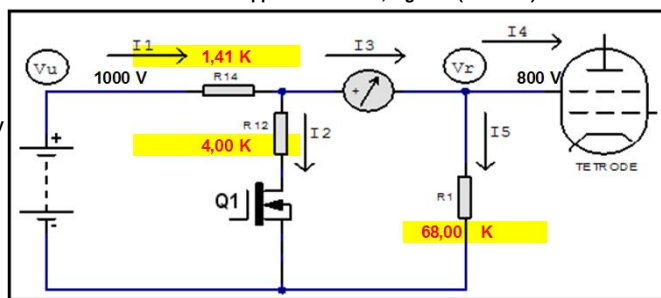
## Calculation of R1, R12, R14

This spreadsheet follows the method described in Application Note 3 © 2003 IFW Technical Services Version 1.0 7 March 2003 by GM3SEK

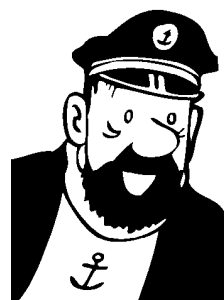
**Modification for F1FRV board, with power MOSFET or IGBT and Q1 & R1 at DC ground**

[http://f1frv.free.fr/main1a\\_Tetrode\\_Linear\\_Amp.html](http://f1frv.free.fr/main1a_Tetrode_Linear_Amp.html)

Application Note 3, Figure 2 (modified)



Input cells are **Black** Results are **Red**



Rev 2 January 2022

New modified schematic  
Added Q1 VDS min / max display  
Safe Operation Area examples  
for MOSFETs & IGBTs

Step

1 Enter unregulated input voltage: **Vu = 1000 V** at load ~ **142 mA**  
Estimated transformer voltage before rectifiers & filter: **741 V AC**

2 Enter regulated output voltage: **Vr = 800 V**

3 Resistor R1: Use next standard value below **80,00 k**  
Enter value used for R1: **R1 = 68,00 k**  
Power dissipation of R1 **10 W**

4 Enter maximum positive screen current: **I4 = + 100 mA**  
Minimum value of I2 (keep-alive current for Q1) = **10 mA**

5 Resistor R14: Use next standard value below **1,62 k**  
Enter value used for R14: **R14 = 1,41 k**  
Power dissipation of R14 **29 W**

6 Enter maximum negative screen current: **I4 = - 50 mA**

7 Resistor R12: Use next standard value below **4,75 k**  
Enter value used for R12: **R12 = 4,00 k**  
Maximum power dissipation of R12 = **96 W** @ I2 = **168 mA**

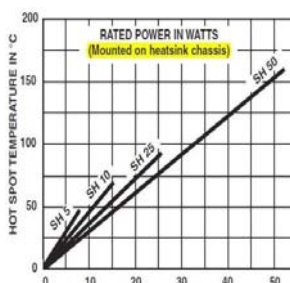
(for Q1 selection) VDS voltage @ Max dissipation = **238 V** @ I2 = **168 mA**  
(for Q1 selection) MAXIMUM current = **168 mA** @ VDS = **238 V**  
(for Q1 selection) MAXIMUM power dissipation = **40 W** @ I2 = **50 mA**  
(for Q1 selection) MAXIMUM VDS voltage @ Min dissipation = **700 V** @ I2 = **100 mA**

Q1 reference (see datasheet) **IGBT FGH30S130P** Q1 Power **500 W** @ 25°C  
Q1 MAXIMUM Power @ Junction Temperature **324 W** Q1 Derating **3,33 W / °C**

Tube:  
**QBL5-3500**



R1, R12 & R14



68 kOhms	R1
25 W	
Values in Figure 2	
I5 =	12 mA
I3 Pos =	112 mA
I1 =	142 mA
I3 Neg =	-38 mA
I2 =	168 mA

4 x 1 kOhms	R12
50 W	

Heatsink thermal resistance **0,7 °C/W**  
Q1 Junction to Case **0,30 °C/W** (see datasheet)  
Insulating pad Rth **0,20 °C/W**  
Ambient temperature: **30 °C**  
Q1 Junction Temperature: **78 °C**

**SELECT RESISTORS MAX DISSIPATION AT LEAST 2 OR 3 x USED POWER DISSIPATION. SEE TEMP VS POWER CURVE, RESISTORS CAN BE PARALLELED TO OBTAIN THE DESIRED VALUE ( EG. 3 x 3,3 K 50 W IN // TO HAVE 1,1 K 150 W ) RESISTORS CAN BE SERIALISED TO OBTAIN THE DESIRED VALUE ( EG. 2 x 470 50 W in SERIE TO HAVE 0,94 K 100 W )**

### DESIGN CHECK

Go back to **Step 1** now, and try a **5% lower** value for Vu. In cell D24, enter **950 V**

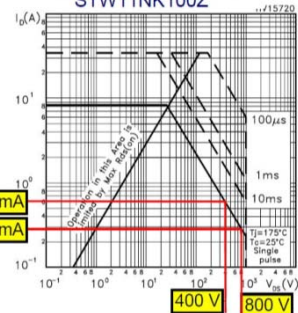
**Do you see any red error messages?**

If you see any red error messages, your present resistor values are marginal!

You should reduce the indicated resistor values, and/or increase the transformer voltage, until **no** error messages appear when you decrease Vu by 5% from your expected minimum value at maximum current. EXCEPT IF YOU ARE SURE OF INPUT VOLTAGE STABILITY AT I1 CURRENT, AND NETWORK MINIMUM VOLTAGE,

Version 1.0 7 March 2003 by GM3SEK **First modification by F1FRV october 2010**

**MOSFET**  
**Safe operating area**  
**STW11NK100Z**



**MOSFET**

Fig. 11. Forward-Bias Safe Operating Area

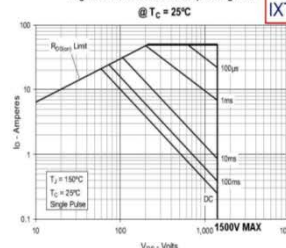
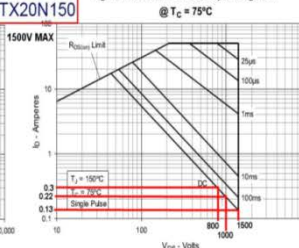


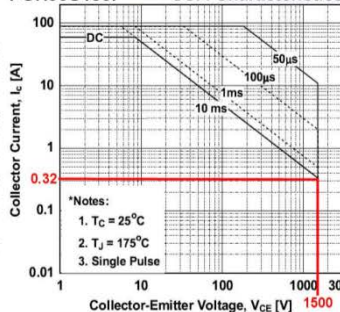
Fig. 12. Forward-Bias Safe Operating Area



**IGBT**

**FGH30S150P**

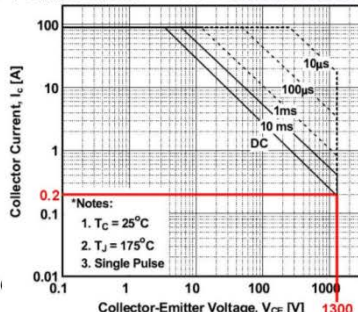
**SOA Characteristics**



**IGBT**

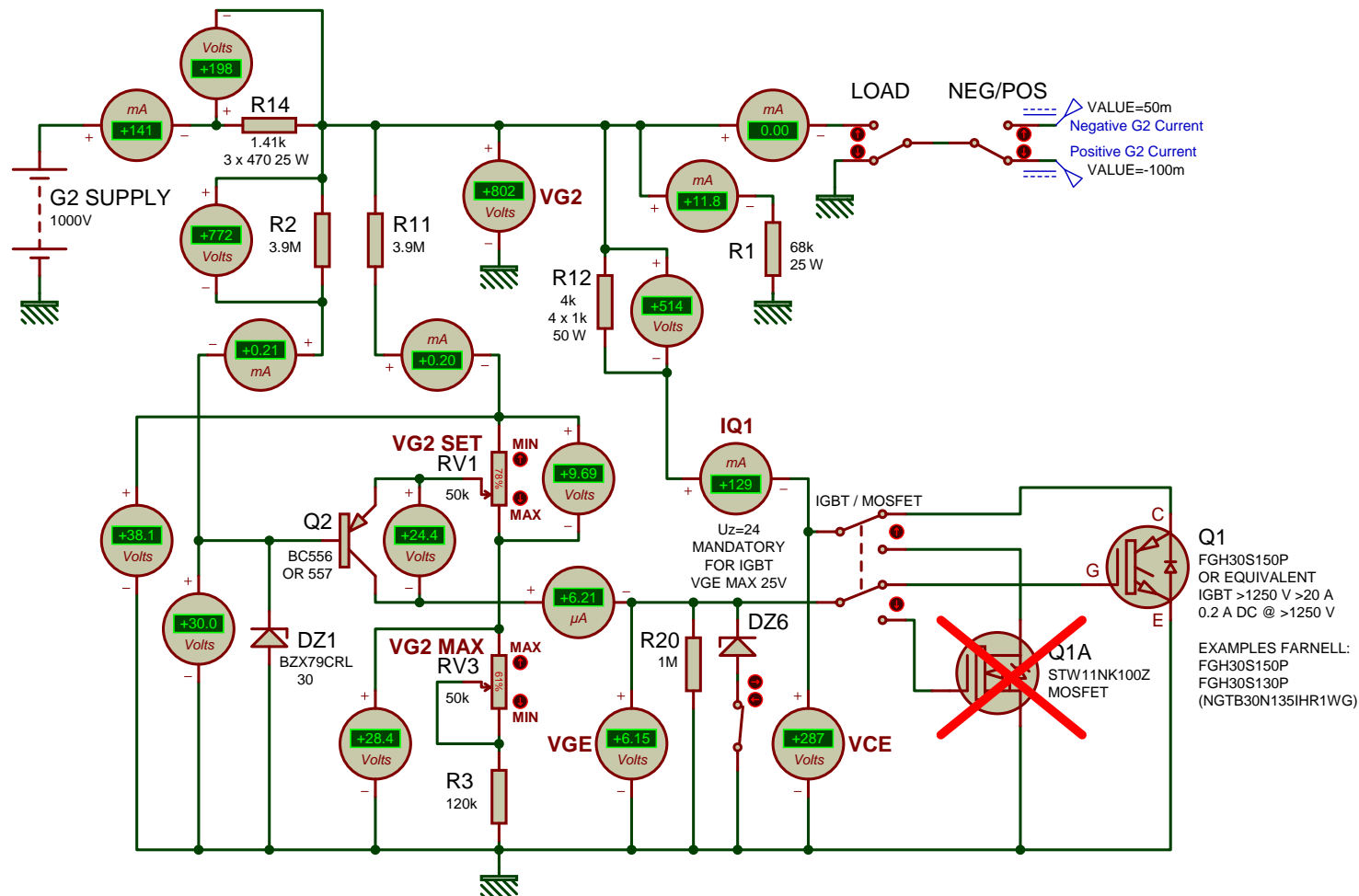
**FGH30S130P**

**SOA Characteristics**



**AS HIGH VOLTAGE MOSFETs FOR G2 > 800 V ARE DIFFICULT TO FIND, USE IGBTs , LESS EXPANSIVES & MORE EASY TO APPROVE.**

**NOTES** If the simulation aborts with "timestep too small" then set : RELTOL=0.005 (up to 0.01) , ITL4=300 (up to 500) , ITL1=300  
And in extreme cases (in order of importance) : GMIN=1e-09 , ABSTOL=1e-08 , VNTOL=1e-05 (up to 1e-03) only if required TMAX=10 t



FOR R1, R12 & R14 VALUES, USE EXCEL SHEET: Grid2\_G3SEK\_an-3-v1.0\_Mod\_F1FRV

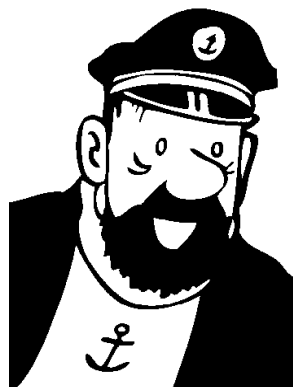
**Simulation files are in "PROTEUS" format. To help you in your design, If you have PROTEUS & want receive simulation files, request by e-mail.**

**EXAMPLE FOR QBL5-3500 WITH G2 : 800 V**

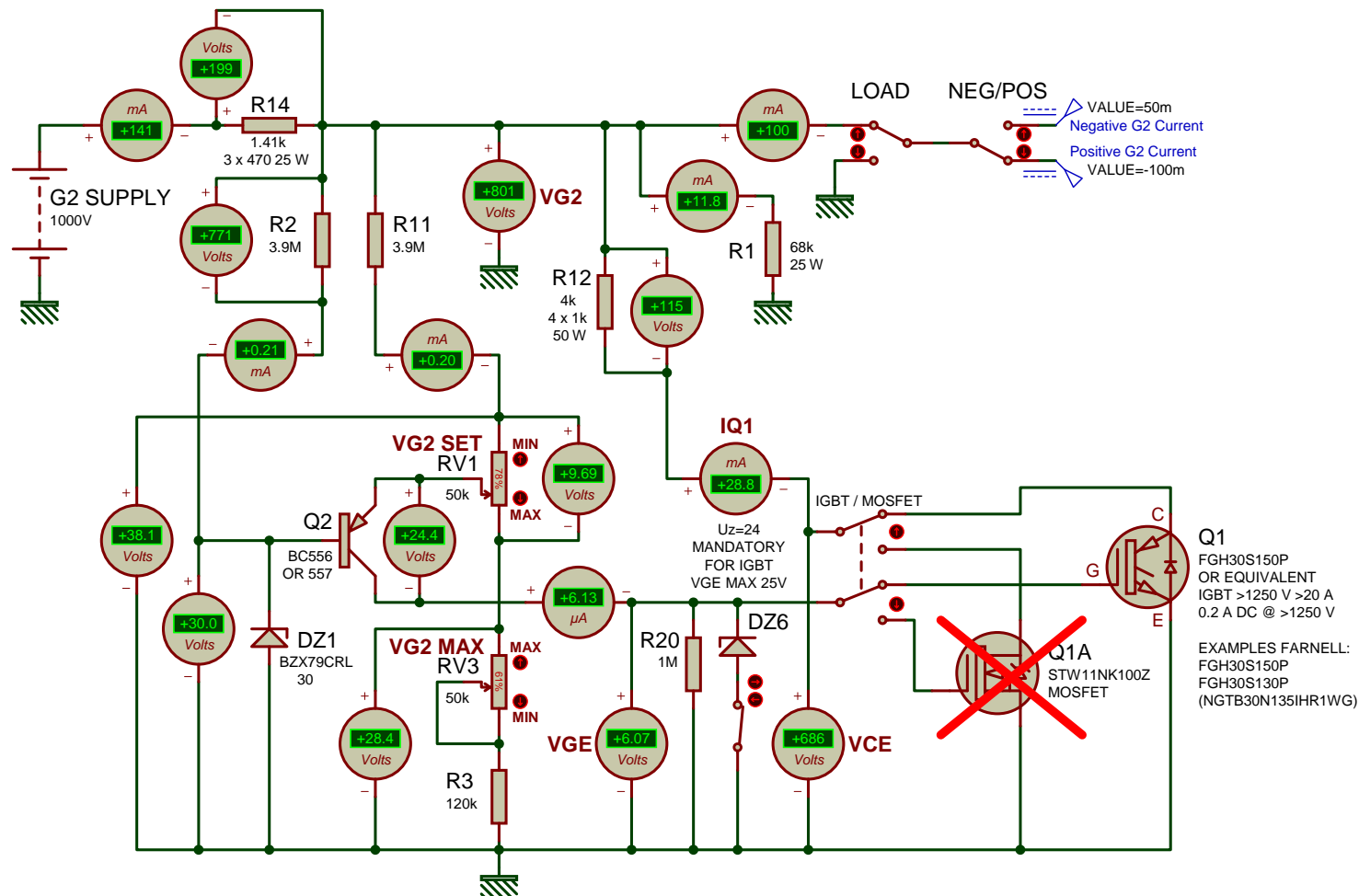
**V G2 800 V (740 V TO 860 V) +100 / -50 mA MAX With IGBT (MANDATORY)**

TETRODE AMPLIFIER DESIGN SUITE  
SIMULATION G2 SHUNT SUPPLY CONTROL

DOC N°: Amateur Radio  
BY: f1frv@sfr.fr  
DATE: 27/01/22 REV: 7 PAGE: 1/1



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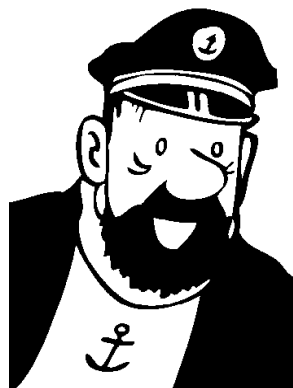
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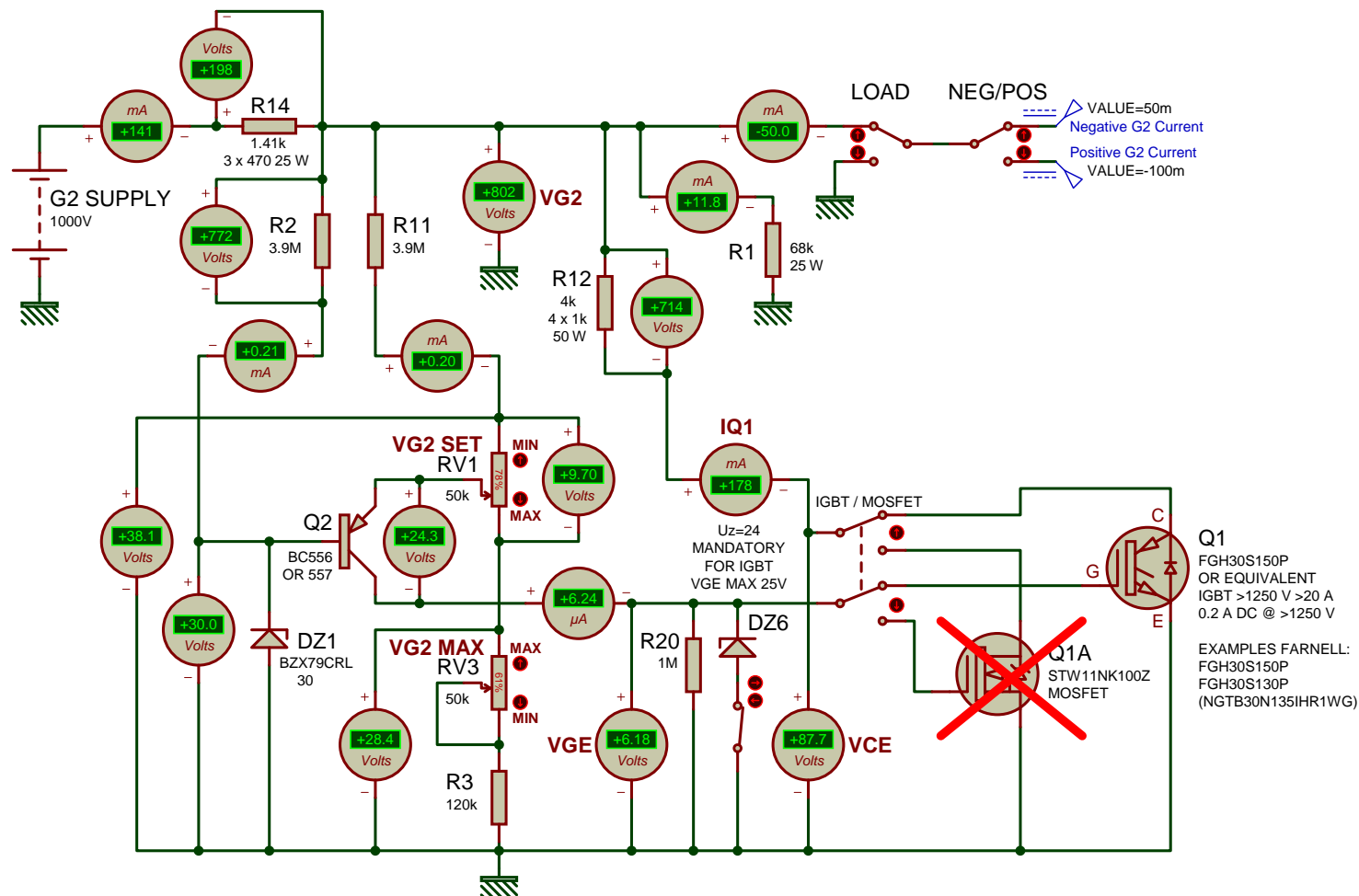
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