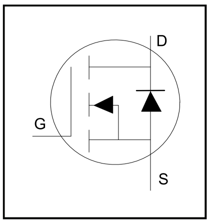
International
IOR Rectifier

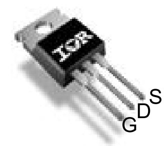
StrongIRFET™
IRF200B211

HEXFET® Power MOSFET

Application
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- DC/DC and AC/DC converters
- DC/AC Inverters



V_{DSS}		200V
$R_{DS(on)}$	typ.	135mΩ
	max	170mΩ
$I_{D\ (Silicon\ Limited)}$		12A



TO-220AB
IRF200B211

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free*, RoHS Compliant, Halogen-Free

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF200B211	TO-220	Tube	50	IRF200B211

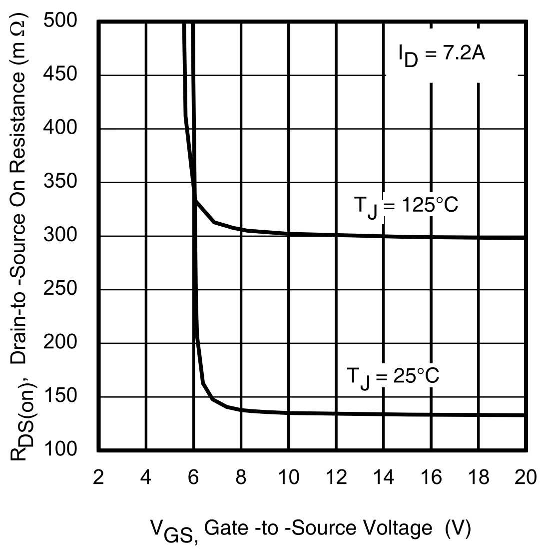


Fig 1. Typical On-Resistance vs. Gate Voltage

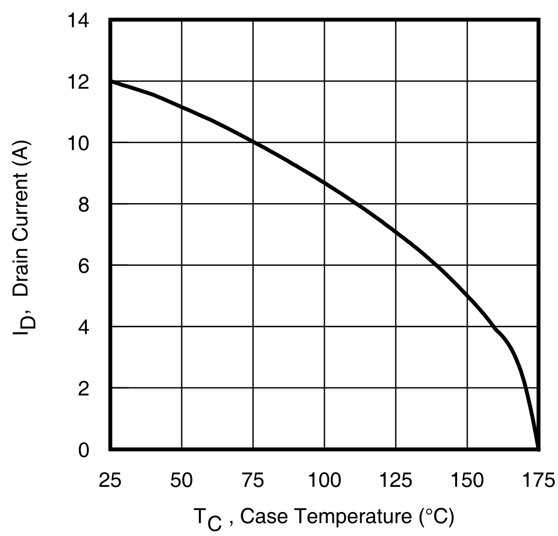


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, VGS @ 10V (Silicon Limited)	12	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	9.0	
I_{DM}	Pulsed Drain Current ②	34	
P_D @T_C = 25°C	Maximum Power Dissipation	80	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	88	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑧	72	
$E_{AS\ (tested)}$	Single Pulse Avalanche Energy Tested Value ⑨	98	
I_{AR}	Avalanche Current ①	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	——	1.88	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.21	——	V/°C	Reference to 25°C, I_D = 1mA ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	135	170	mΩ	V_{GS} = 10V, I_D = 7.2A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	——	4.9	V	V_{DS} = V_{GS}, I_D = 50μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 200V, V_{GS} = 0V
		——	——	250		V_{DS} = 160V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
R_G	Gate Resistance	——	2.7	——	Ω	

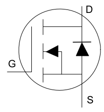
Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Limited by T_{Jmax}, starting T_J = 25°C, L = 3.4mH, R_G = 50Ω, I_{AS} = 7.2A, V_{GS} =10V.
③ $I_{SD} \le$ 7.2A, di/dt $\le$ 1184A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 175°C.
④ Pulse width $\le$ 400μs; duty cycle $\le$ 2%.
⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while VDS is rising from 0 to 80% V_{DSS}.
⑦ R_θ is measured at T_J approximately 90°C.
⑧ Limited by T_{Jmax}, starting T_J = 25°C, L = 1.0mH, R_G = 50Ω, I_{AS} = 11.5A, V_{GS} =10V.
⑨ This value determined from sample failure population, starting T_J = 25°C, L= 3.4mH, R_G = 50Ω, I_{AS} = 7.2A, V_{GS} =10V.

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	13	——	——	S	V_{DS} = 50V, I_D = 7.2A
Q_g	Total Gate Charge	——	15.3	23	nC	I_D = 7.2A
Q_{gs}	Gate-to-Source Charge	——	5.1	——		V_{DS} = 100V
Q_{gd}	Gate-to-Drain Charge	——	5.6	——		V_{GS} = 10V④
Q_{sync}	Total Gate Charge Sync. (Qg– Qgd)	——	10.2	——		
$t_{d(on)}$	Turn-On Delay Time	——	6.5	——	ns	V_{DD} = 130V
t_r	Rise Time	——	9.5	——		I_D = 7.2A
$t_{d(off)}$	Turn-Off Delay Time	——	11.3	——		R_G= 2.7Ω
t_f	Fall Time	——	6.5	——		V_{GS} = 10V④
C_{iss}	Input Capacitance	——	790	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	62	——		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	——	21	——		f = 1.0MHz, See Fig.TBD
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	——	66	——		V_{GS} = 0V, VDS = 0V to 160V⑥
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	——	83	——		V_{GS} = 0V, VDS = 0V to 160V⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	12	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	34		
V_{SD}	Diode Forward Voltage	——		1.3	V	T_J = 25°C, I_S = 7.2A,V_{GS} = 0V ④
dv/dt	Peak Diode Recovery dv/dt③	——	32.5	——	V/ns	T_J =175°C,I_S = 7.2A,V_{DS} = 200V
t_{rr}	Reverse Recovery Time	——	68	——	ns	T_J = 25°C V_{DD} = 100V
		——	83	——		T_J = 125°C I_F = 7.2A,
Q_{rr}	Reverse Recovery Charge	——	195	——	nC	T_J = 25°C di/dt = 100A/μs ④
		——	280	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	4.3	——	A	T_J = 25°C

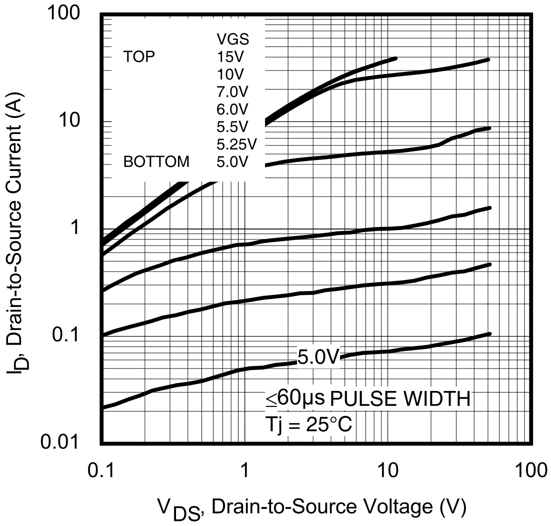


Fig 3. Typical Output Characteristics

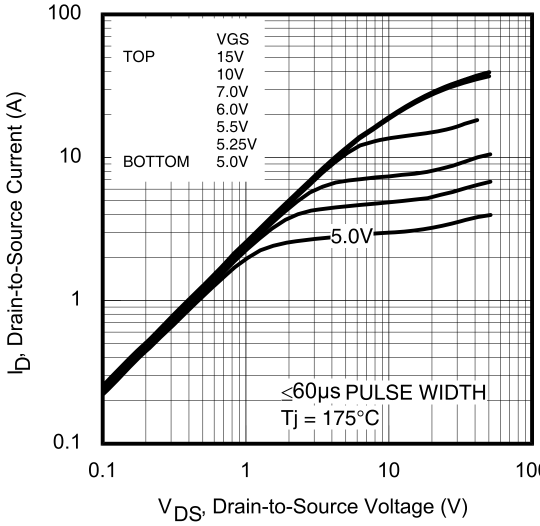


Fig 4. Typical Output Characteristics

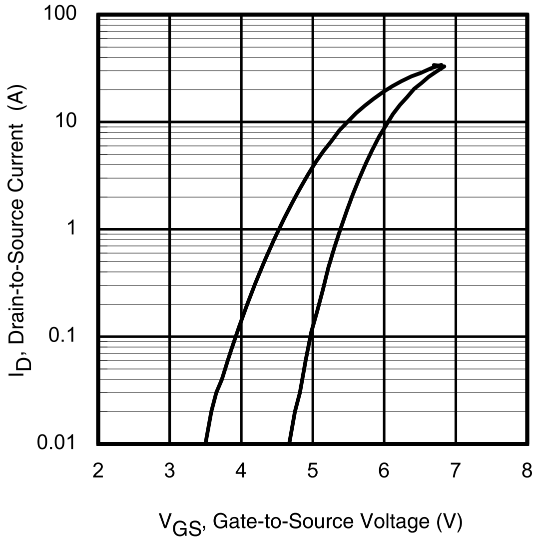


Fig 5. Typical Transfer Characteristics

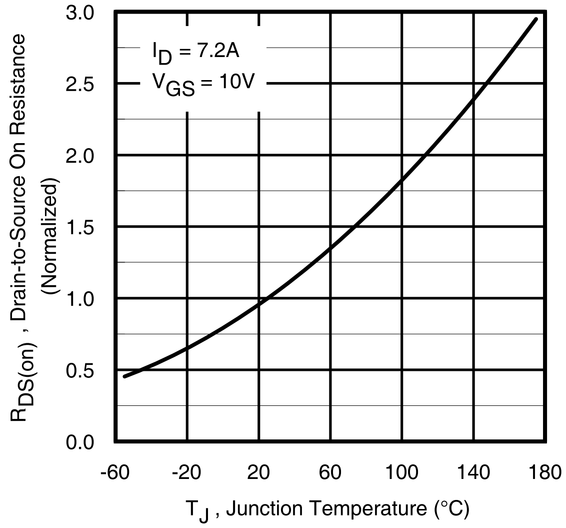


Fig 6. Normalized On-Resistance vs. Temperature

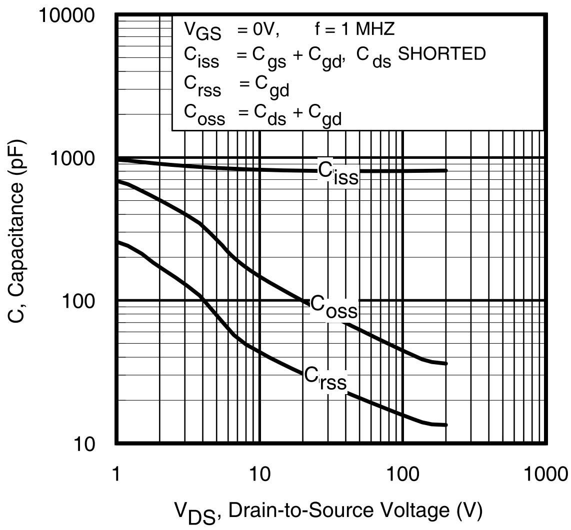


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

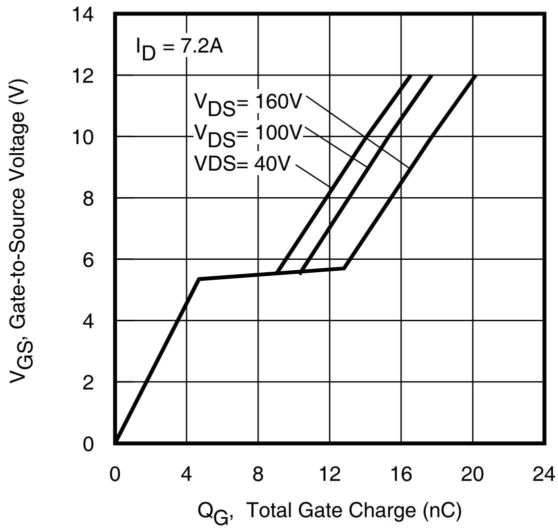


Fig 8. Typical Gate Charge vs.Gate-to-Source Voltage

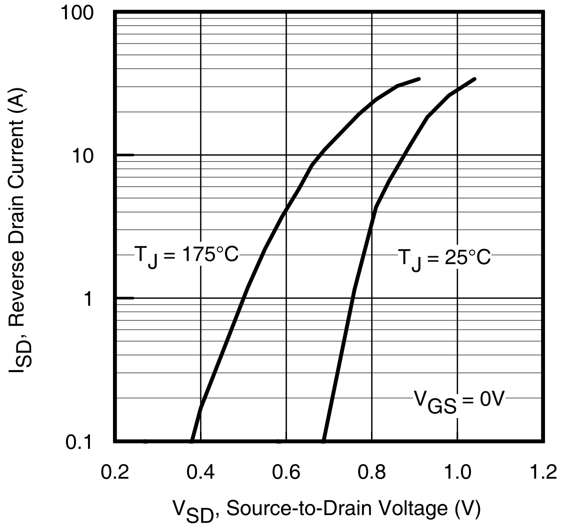


Fig 9. Typical Source-Drain Diode Forward Voltage

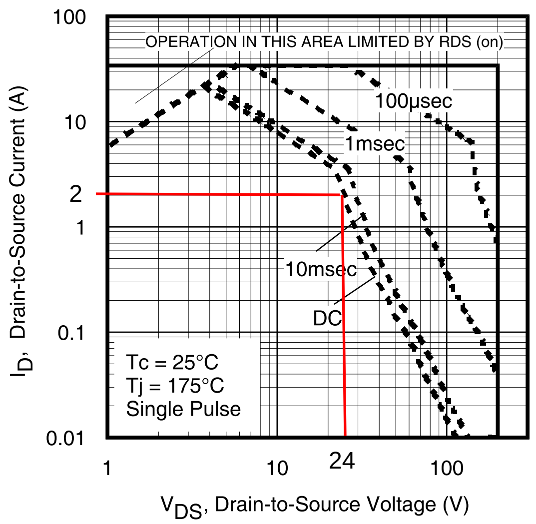


Fig 10. Maximum Safe Operating Area

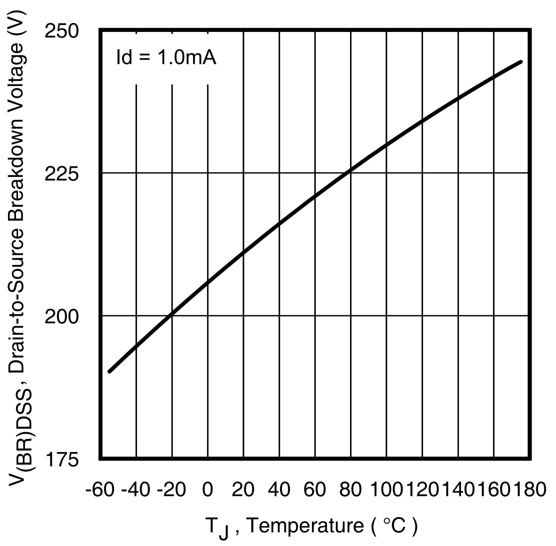


Fig 11. Drain-to-Source Breakdown Voltage

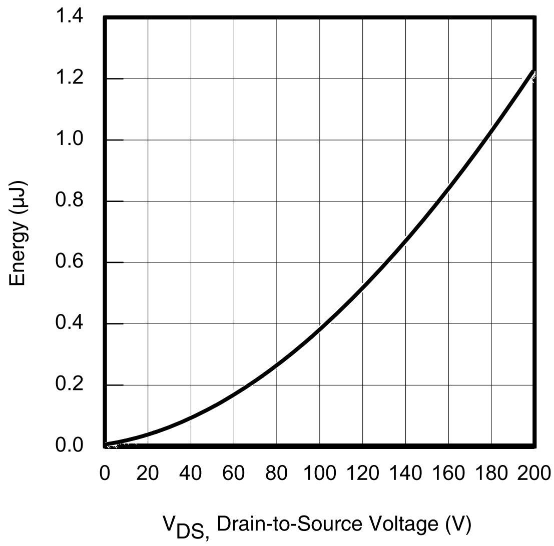


Fig 12. Typical C_{oss} Stored Energy

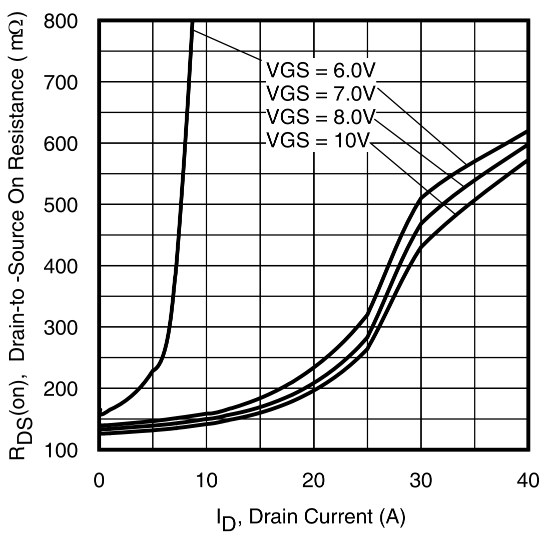


Fig 13. Typical On– Resistance vs. Drain Current

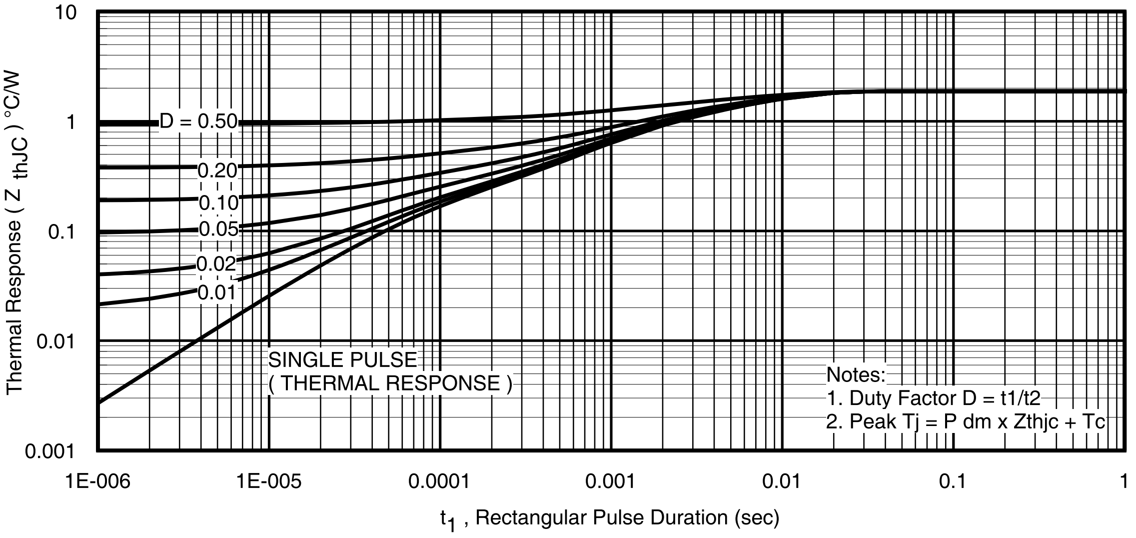


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

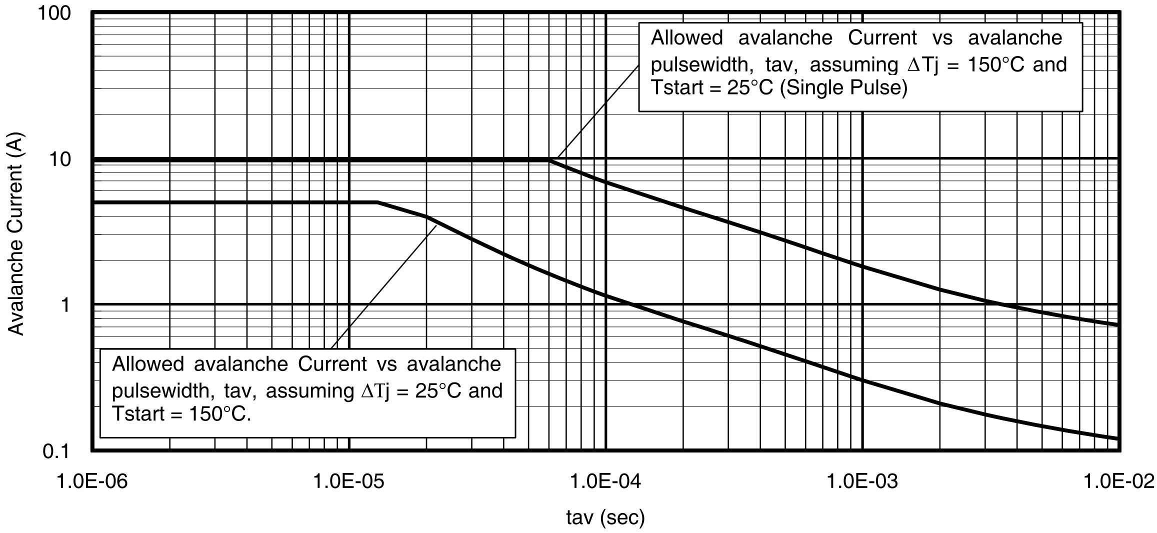


Fig 15. Avalanche Current vs. Pulse Width

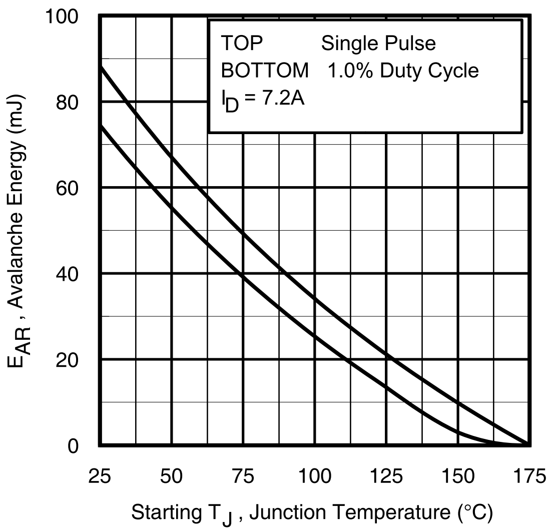


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

$$PD\ (ave) = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

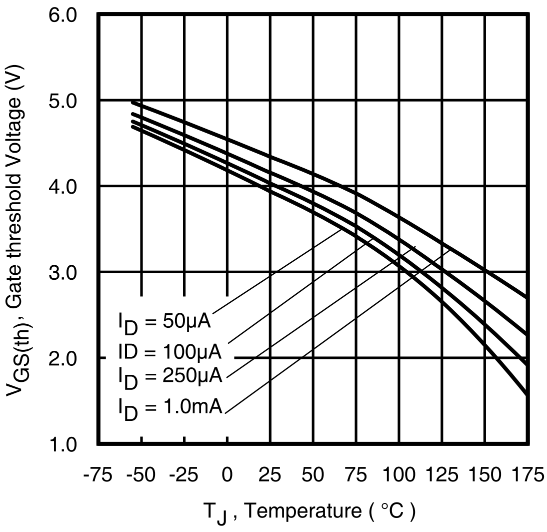


Fig 17. Threshold Voltage vs. Temperature

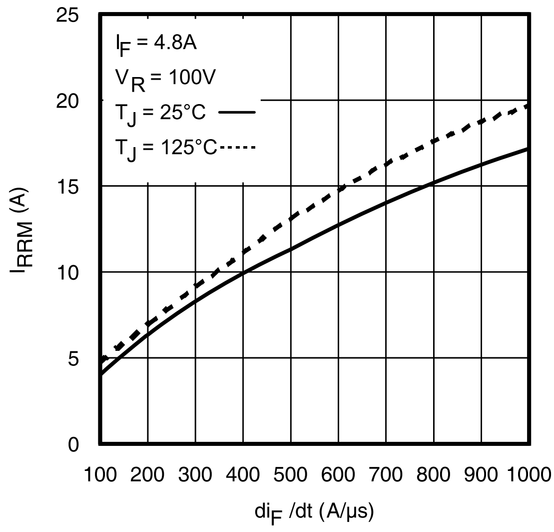


Fig 18. Typical Recovery Current vs. dif/dt

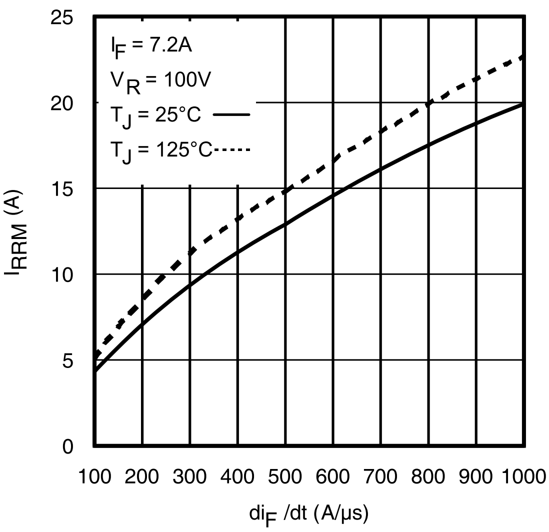


Fig 19. Typical Recovery Current vs. dif/dt

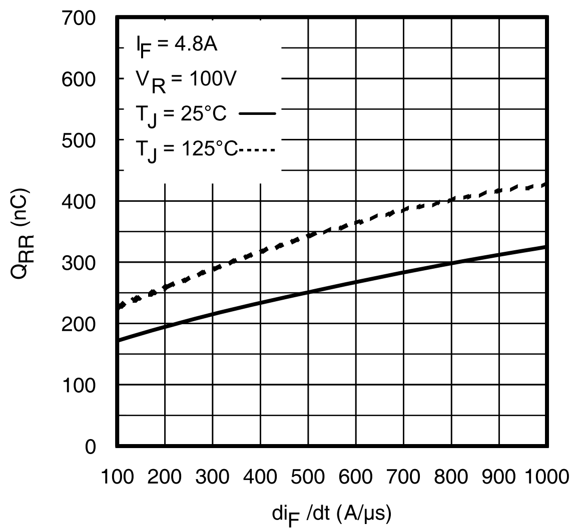


Fig 20. Typical Stored Charge vs. dif/dt

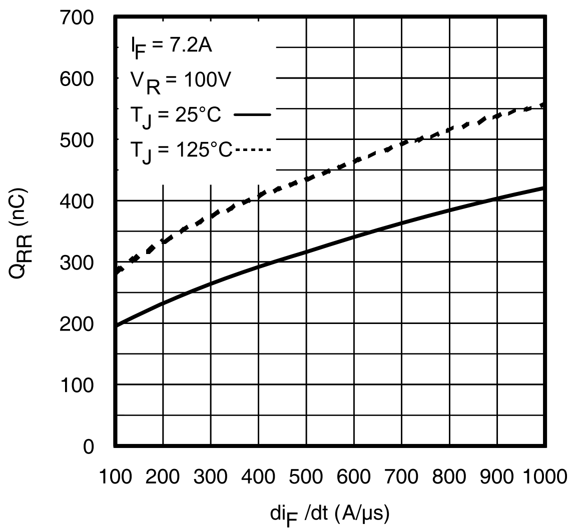


Fig 21. Typical Stored Charge vs. dif/dt

