TEXAS INSTRUMENTS - CD74AC04E - CIRCUIT LOGIQUE SERIE 74AC

Image non contractuelle - Seulement à titre d illustration. Veuillez vous reporter au descriptif technique.

Fabricant: TEXAS INSTRUMENTS

Code commande: 1102987

Référence fabricant: CD74AC04E

Conformité RoHS : **Oui**

Description

- CIRCUIT LOGIQUE SERIE 74AC
- Nombre d'entrées:1
- Type de boîtier CI logique:DIP
- Nombre de broches:14
- Température de fonctionnement:-55°C à +125°C
- SVHC:No SVHC
- Type de boîtier:DIP
- Courant, sortie max.:24mA
- Famille Circuit logique:AC
- Fonction logique:Six inverseurs
- Nombre de portes:6
- Numéro de base de la fonction logique:7404
- Numéro de la fonction logique:04
- Numéro générique:74AC04
- Racine de la référence:74
- Température de fonctionnement max.:125°C
- Température de fonctionnement min.:-55°C
- Tension, alimentation:5.5V
- Tension, alimentation maxi:5.5V
- Tension, alimentation mini:1.5V
- Type de terminaison:Traversant

Afficher les Accessoires

Disponibilité

Disponibilité: 176

Prix Pour: 1 Pièce

Quantité minimum: 1

Multiple de commande: 1

Prix Unitaire HT: 0,63 €

Qté 1

Prix

Qté	Prix Unitaire HT
1 - 9	0,63 €
10 - 99	0,40 €
100 - 499	0,29 €
500+	0,21 €

Accessoires

SUPPORT CI DIL 7.62MM 14VOIES
MULTICOMP 2227MC-14-03-10-F1

1 Pièce
0,74 €

TESTER, COUNTERFEIT IC DETECTOR, SENTRY
ABI 603082

1 Pièce
2 821,00 €

CIRCUIT TESTEUR NUMERIQUE (SANS ADAPT)
LEAP ELECTRONIC LP-1

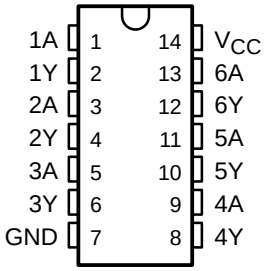
1 Pièce
157,96 €

Nos clients ont aussi acheté

DESCRIPTION TECHNIQUE	ATTRIBUTS TECHNIQUES	EQUIVALENT
Certificat de conformité RoHS Manufacturer Product Page (87.89KB) EN Technical Data Sheet (508.51KB)	**poids (kg):** 0.002 **Tarif Douanier:** 85423990 **Pays d'origine:** MY Malaisie *Pays dans lequel la dernière étape de production majeure*	Nombre d'entrées: 1 Type de boîtier CI logique: DIP Nombre de broches: 14 Température de fonctionnement: -55°C à

- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **±24-mA Output Drive Current**
  – Fanout to 15 F Devices
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

CD54AC04 . . . F PACKAGE
CD74AC04 . . . E OR M PACKAGE
(TOP VIEW)



description

The ‘AC04 devices contain six independent inverters. The devices perform the Boolean function $Y = \overline{A}$.

ORDERING INFORMATION

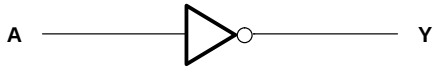
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74AC04E	CD74AC04E
	SOIC – M	Tube	CD74AC04M	AC04M
		Tape and reel	CD74AC04M96	
	CDIP – F	Tube	CD54AC04F3A	CD54AC04F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package . . . . . 80°C/W
M package . . . . . 86°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			T_A = 25°C		–40°C TO 85°C		–55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 1.5 V	1.2		1.2		1.2		V
		V_{CC} = 3 V	2.1		2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 1.5 V		0.3		0.3		0.3	V
		V_{CC} = 3 V		0.9		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.5 V to 5.5 V		–24		–24		–24	mA
I_{OL}	Low-level output current	V_{CC} = 4.5 V to 5.5 V		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.5 V to 3 V		50		50		50	ns/V
		V_{CC} = 3.6 V to 5.5 V		20		20		20	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		−40°C TO 85°C		−55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –50 μA	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58		2.48		2.4		
		I_{OH} = –24 mA	4.5 V	3.94		3.8		3.7		
		I_{OH} = –50 mA†	5.5 V					3.85		
		I_{OH} = –75 mA†	5.5 V			3.85				
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 50 μA	1.5 V		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V		0.36		0.44		0.5	
		I_{OL} = 24 mA	4.5 V		0.36		0.44		0.5	
		I_{OL} = 50 mA†	5.5 V						1.65	
		I_{OL} = 75 mA†	5.5 V				1.65			
I_I	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V		4		40		80	μA
C_i					10		10		10	pF

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−40°C TO 85°C		−55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y		74		81	ns
t_{PHL}				74		81	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−40°C TO 85°C		−55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.3	8.3	2.3	9.1	ns
t_{PHL}			2.3	8.3	2.3	9.1	

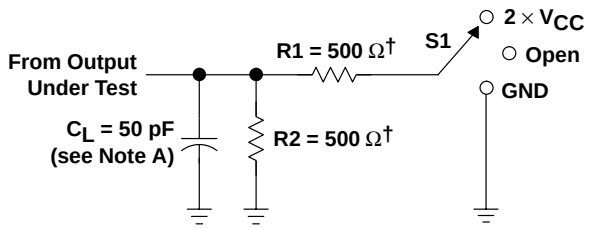
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 85°C		–55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.7	5.9	1.6	6.5	ns
t_{PHL}			1.7	5.9	1.6	6.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	105	pF

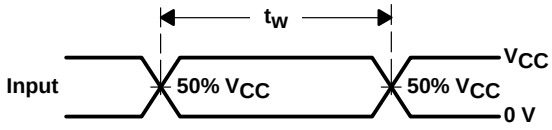
PARAMETER MEASUREMENT INFORMATION



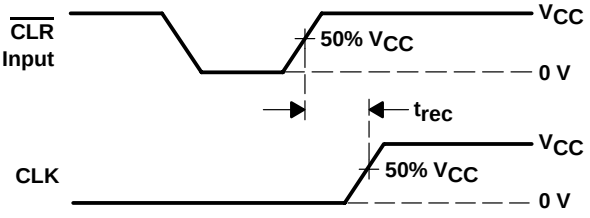
† When V_{CC} = 1.5 V, R1 = R2 = 1 kΩ

LOAD CIRCUIT

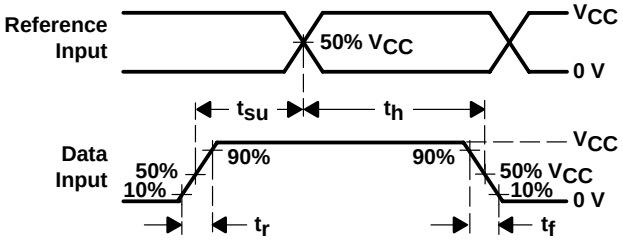
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



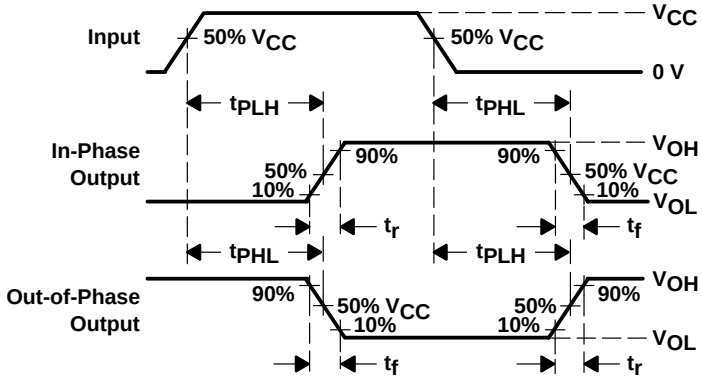
VOLTAGE WAVEFORMS
PULSE DURATION



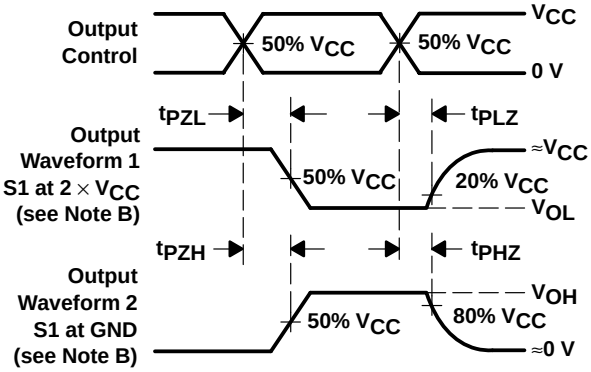
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Figure 1. Load Circuit and Voltage Waveforms